

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1 Claim 1. (*Currently Amended*) A decoder for decoding encoded data, the decoder
2 comprising:

3 a processor having an input which receives probability estimates for a block of symbols,
4 and which is arranged to calculate probability estimates for said symbols in a next iterative state;

5 ~~normalising means which normalises said next states~~ normalizing means for normalizing
6 said calculated probability estimates to provide normalized probability estimates;

7 a switch ~~that receives both said normalised and said unnormalised next state~~ arranged to
8 receive both said calculated probability estimates and said normalized probability estimates,
9 [[the]] an output of the switch being coupled to the input of the processor;

10 wherein the switch is arranged to switch between the ~~normalised and unnormalised next~~
11 state calculated probability estimates and the normalized probability estimates depending on the
12 iterative state.

1 Claim 2. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein said
2 decoder comprises a MAP algorithm wherein the probability estimates are α and β values.

1 Claim 3. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein said
2 decoder has eight iterative states for each received symbol block.

1 Claim 4. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein the ratio
2 between said ~~unnormalised and said normalised next state~~ calculated probability estimates and
3 said normalized probability estimates is 7:1.

1 Claim 5. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein said
2 switch is a multiplexer.

1 Claim 6. (*Currently Amended*) [[A]] The decoder according to claim 1 further comprising
2 pipeline registers between said processor and said ~~normalising~~ normalizing function.

1 Claim 7. (*Currently Amended*) A turbo decoder comprising [[a]] the decoder according to
2 claim 1.

1 Claim 8. (*Currently Amended*) A decoder for decoding encoded data, the decoder
2 comprising:

3 a processor having an input which receives probability estimates for a block of symbols,
4 and which is arranged to calculate probability estimates for said symbols in a next iterative state;
5 ~~normalising~~ normalizing means coupled to the processor ~~which normalises said next state~~
6 for normalizing said calculated probability estimates to provide normalized probability estimates;
7 ~~wherein the decoder further comprises~~ pipelining means between the processor and the
8 ~~normalising~~ normalizing means for providing ~~non-normalised next state~~ non-normalized
9 probability estimates; and
10 switching means for receiving both said calculated probability estimates and said
11 normalized probability estimates, an output of the switching means being coupled to the input of
12 the processor;
13 wherein the switching means is arranged to switch between the calculated probability
14 estimates and the normalized probability estimates depending on the iterative state.

Claim 9 (*Canceled*)

1 Claim 10. (*Currently Amended*) [[A]] The decoder according to claim 8 wherein said
2 pipelining means is a pipeline register coupled between outputs of said processor and inputs of
3 said ~~normalising~~ normalizing means.